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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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#8

Stephanie Daryaie
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Applicant : Mathieu Tallegas, et al.
Application No. : 09/757,361
Filed : January 8, 2001
Title : PACKET PROCESSOR WITH MULTI-LEVEL
POLICING LOGIC
Grp./Div. : 2661
Examiner : To be assigned
Docket No. : 40032/JEJ/X2

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
37 CFR § 1.97(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Post Office Box 7068
Pasadena, CA 91109-7068
June 24, 2002

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, and in accordance with the provisions in the Manual of Patent Examining Procedure §§ 609 and 707.05(b), enclosed is FORM PTO/SB/08A/B listing the references that are known to applicant. Copies of each of the listed references are enclosed. This filing is timely because it is made during one of the periods described in 37 CFR § 1.97(b).

It is respectfully requested that the listed references be considered in the examination of this application and identified on the list of references cited on the patent issuing for this application. Applicant also requests that an initialed copy of FORM PTO/SB/08A/B be entered in the application file and returned to applicant with the next communication from the Office in accordance with MPEP § 609.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

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626/795-9900

JEJ/sd

Enclosures: PTO/SB/08A/B, w/references
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